NEC

MOS FIELD EFFECT TRANSISTOR

NP34N055HHE, NP34N055IHE

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

These products are N-Channel MOS Field Effect Transistors designed for high current switching applications.

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance
  $R_{DS(on)}$ = 19 mΩ MAX. (V_{GS} = 10 V, I_D = 17 A)
- Low C_{iss} : C_{iss} = 1600 pF TYP.
- Built-in gate protection diode

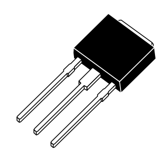
ORDERING INFORMATION

PART NUMBER	PACKAGE
NP34N055HHE	TO-251
NP34N055IHE	TO-252

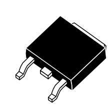
ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage	V_{DSS}	55	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±34	A
Drain Current (Pulse) Note1	$I_{D(pulse)}$	±136	A
Total Power Dissipation (T_A = 25 °C)	P_T	1.2	W
Total Power Dissipation (T_C = 25 °C)	P_T	88	W
Single Avalanche Current Note2	I_{AS}	34 / 27 / 10	A
Single Avalanche Energy Note2	E_{AS}	11 / 72 / 100	mJ
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to + 175	°C

(TO-251)



(TO-252)



Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1 %

2. Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0 V (see Figure 4.)

THERMAL RESISTANCE

Channel to Case	$R_{th(ch-C)}$	1.70	°C/W
Channel to Ambient	$R_{th(ch-A)}$	125	°C/W

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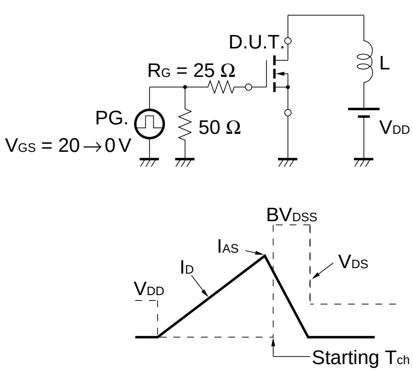
The mark ★ shows major revised points.

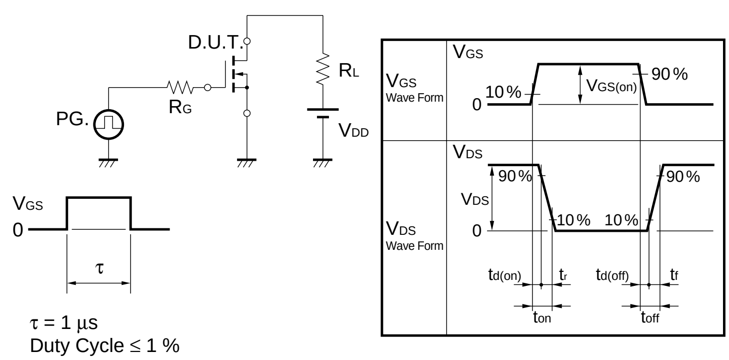
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 17 A		15	19	mΩ
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	3.0	4.0	V
Forward Transfer Admittance	$\vert y_{fs} \vert$	V_{DS} = 10 V, I_D = 17 A	6	12		S
Drain Leakage Current	I_{DSS}	V_{DS} = 55 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 25 V		1600	2400	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		250	380	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		120	220	pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 17 A		21	47	ns
Rise Time	t_r	$V_{GS(on)}$ = 10 V		15	38	ns
Turn-off Delay Time	$t_{d(off)}$	V_{DD} = 28 V		35	70	ns
Fall Time	t_f	R_G = 1 Ω		12	29	ns
Total Gate Charge	Q_G	I_D = 34 A		30	45	nC
Gate to Source Charge	Q_{GS}	V_{DD} = 44 V		9		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 10 V		12		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 34 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 34 A, V_{GS} = 0 V		40		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		58		nC

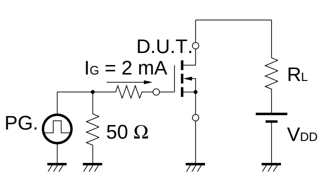
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS (T_A = 25°C)

Figure1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

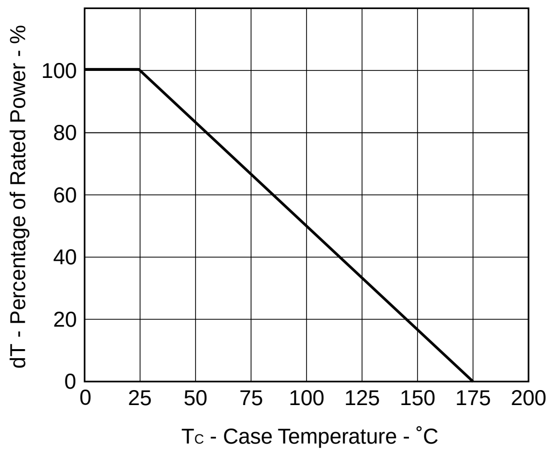
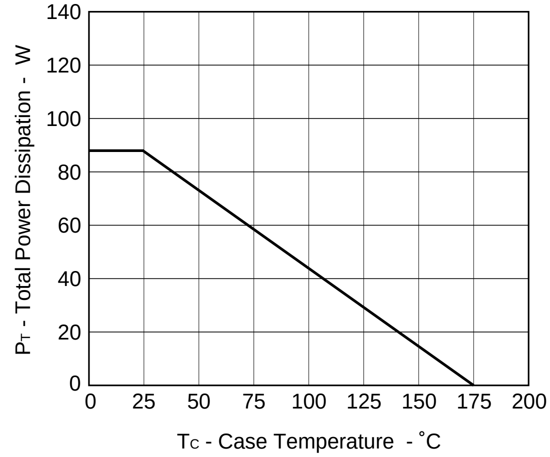


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



★ Figure3. FORWARD BIAS SAFE OPERATING AREA

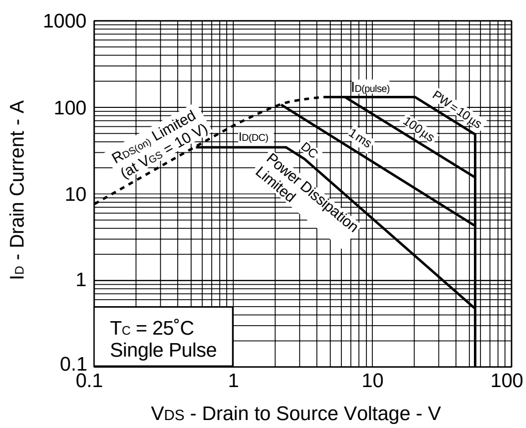


Figure4. SINGLE AVALANCHE ENERGY DERATING FACTOR

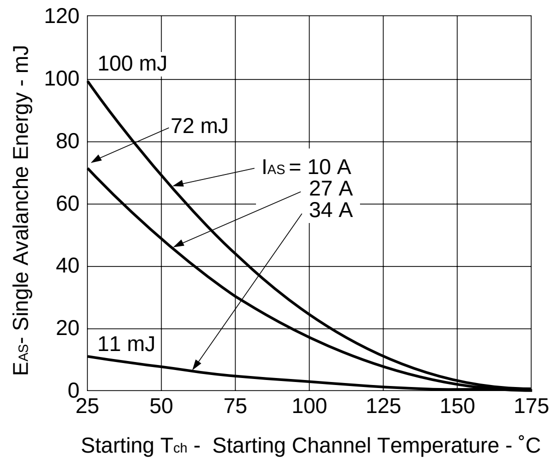


Figure5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

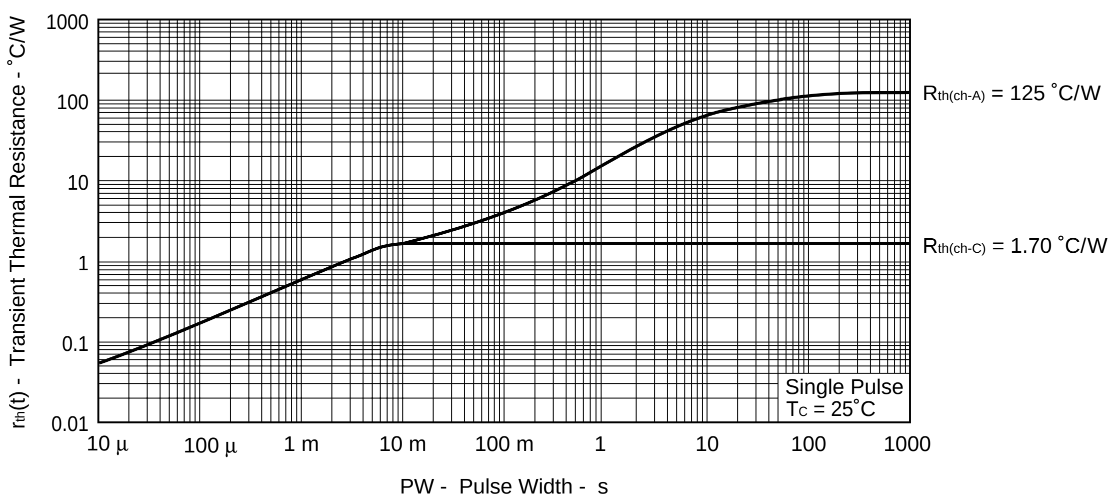


Figure6. FORWARD TRANSFER CHARACTERISTICS

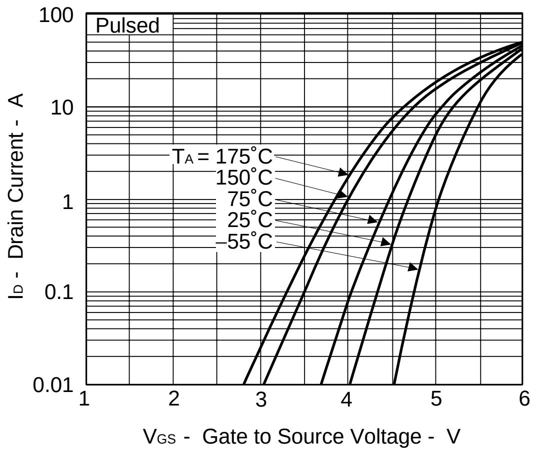


Figure7. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

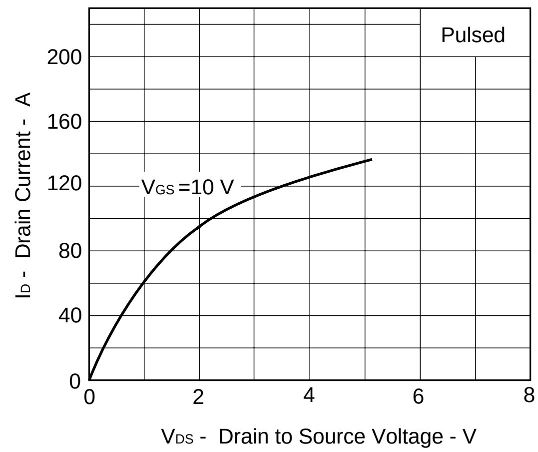


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

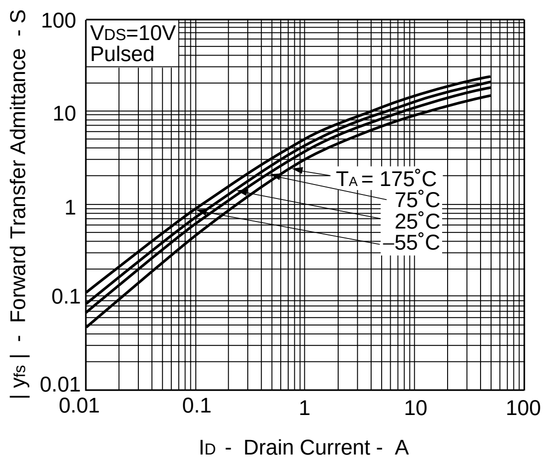


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

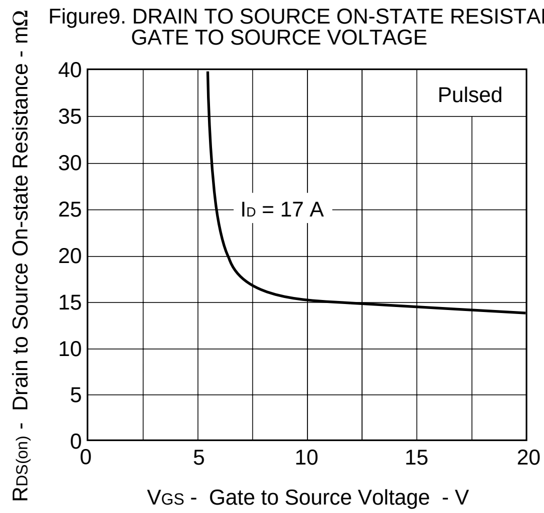


Figure10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

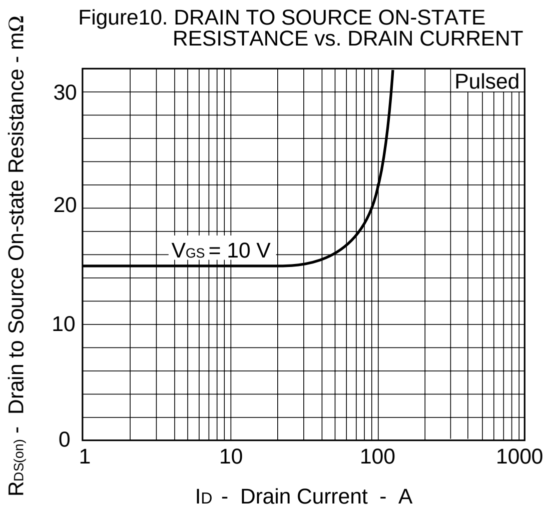


Figure11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

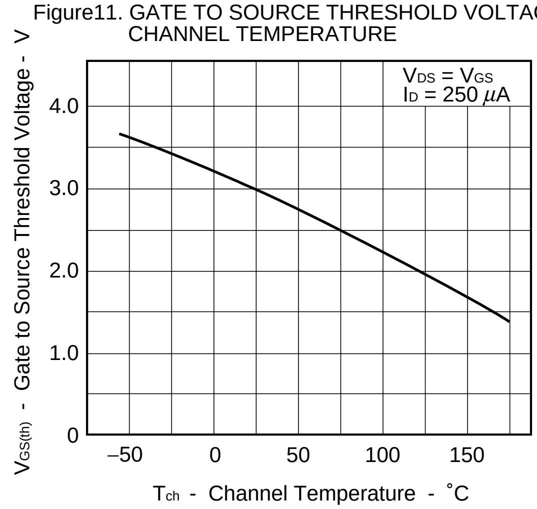


Figure12. DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

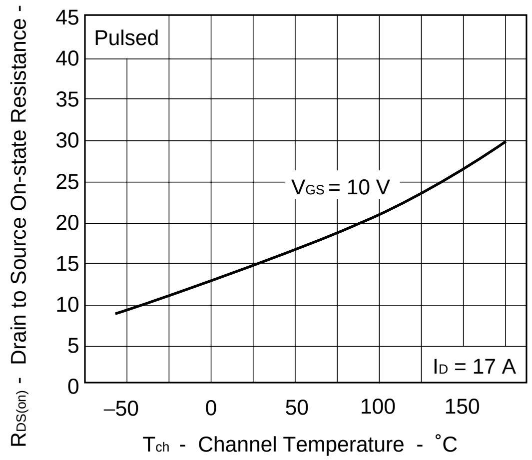


Figure13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

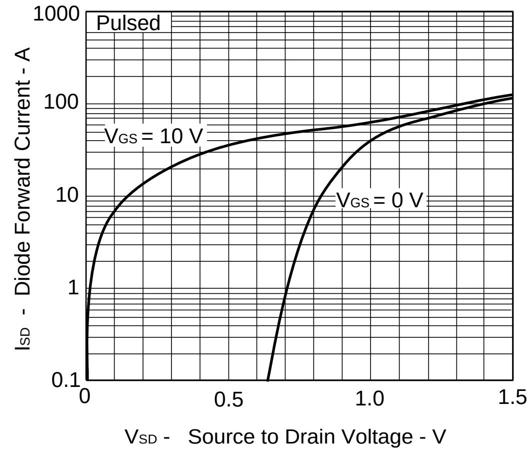


Figure14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

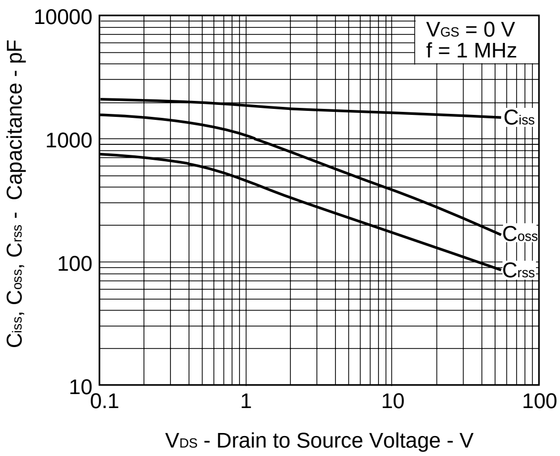


Figure15. SWITCHING CHARACTERISTICS

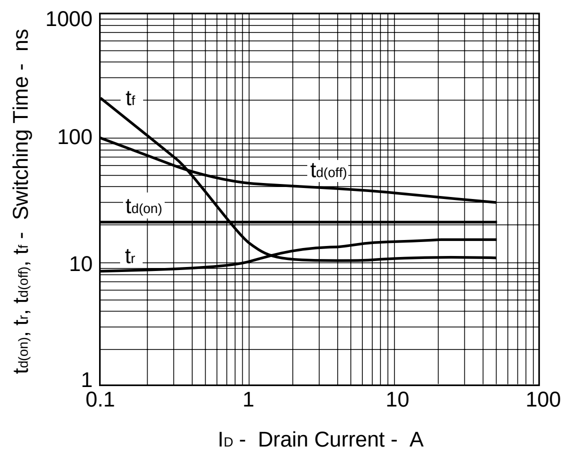


Figure16. REVERSE RECOVERY TIME vs. DRAIN CURRENT

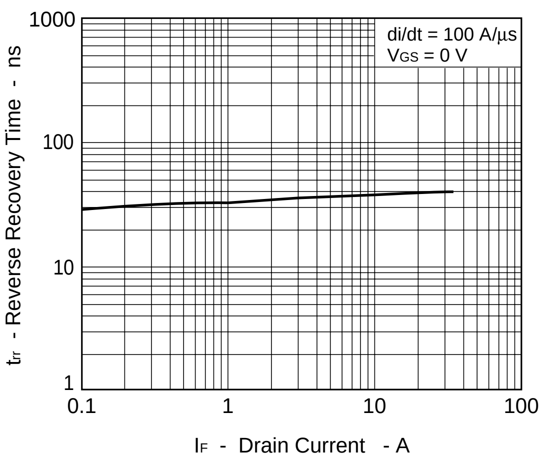
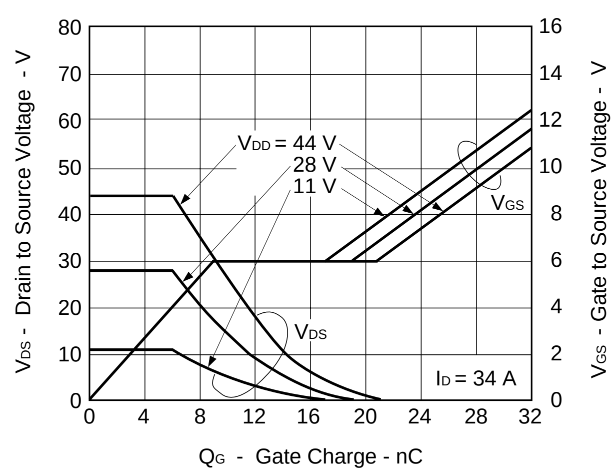
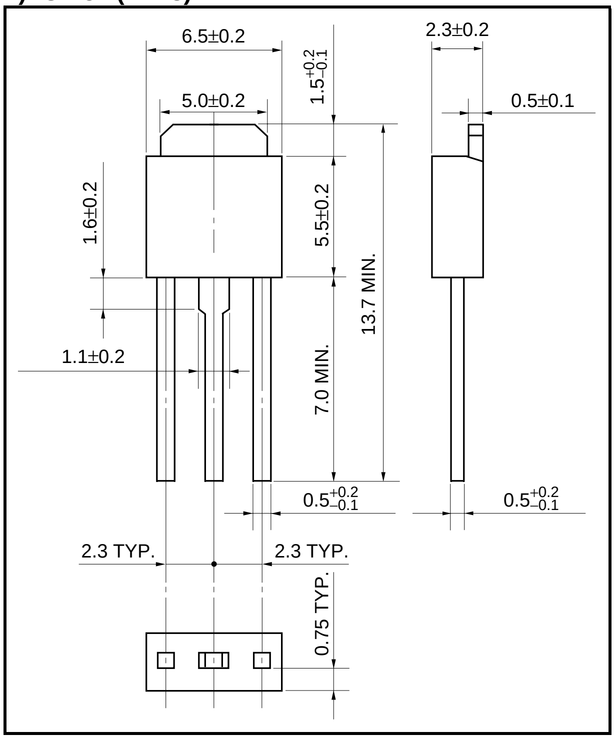


Figure17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

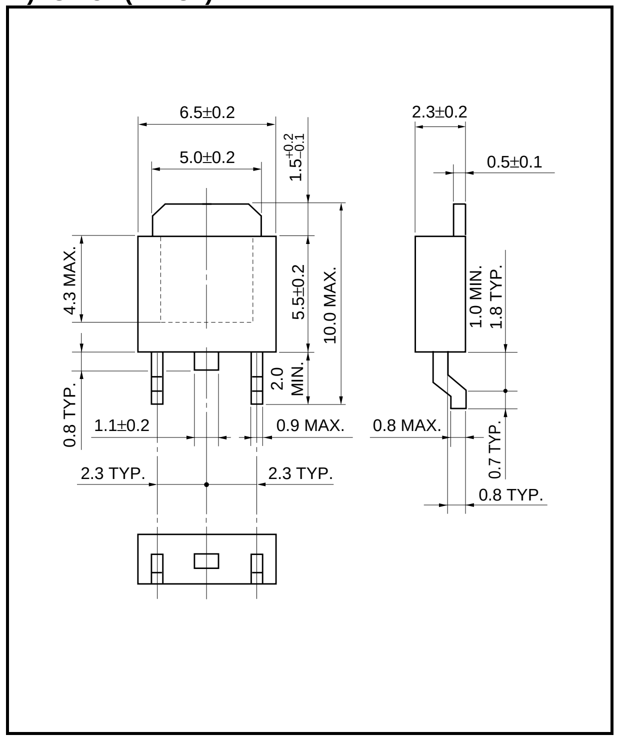


PACKAGE DRAWINGS (Unit : mm)

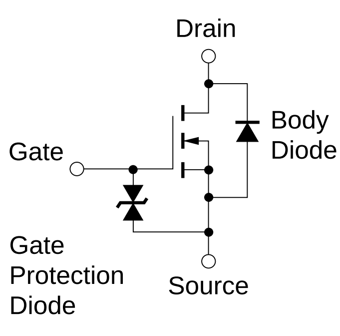
1)TO-251 (MP-3)



2)TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]